## In the Claims:

Please amend claims 4, 7, 13, 14 and 17 as indicated below.

1. (Original) A resource access control mechanism for a computer system including at least one central processing unit, the resource access control mechanism comprising

an address translation mechanism operable to map a received address to a resource and

a trap handler for handling a trap in the event of a faulty resource access being detected, the trap handler being operable to instigate a diversion for subsequent access attempts to the resource and

the address translation mechanism being responsive to instigation of a diversion by the trap handler to effect the diversion for subsequent attempts to access the resource.

- 2. (Original) The resource access control mechanism of claim 1, wherein the trap handler is further operable to process an exception.
- 3. (Original) The resource access control mechanism of claim 1, wherein the address translation mechanism includes a translation look-aside buffer.
- 4. (Currently amended) The resource access control mechanism of claim 1, wherein the address translation mechanism forms part of a memory management unit.
- 5. (Original) The resource access control mechanism of claim 1, wherein the trap handler is operable to identify an alternative resource address to the address translation



mechanism for replacing a resource address held in an address translation entry for the resource.

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- 6. (Original) The resource access control mechanism of claim 1, wherein the trap handler is operable to instigate the diversion by signaling the address translation mechanism.
- 7. (Currently amended) The resource access control mechanism of claim 6, wherein the address translation mechanism is responsive to instigation of a diversion by the trap handler to replace a resource address held in an address translation entry for the resource with an address for an alternative resource address.
- 8. (Original) The resource access control mechanism of claim 6, wherein the address translation mechanism is responsive to instigation of a diversion by the trap handler to set a divert flag in a translation entry of the address translation and is further operable to respond to a received address relating to an address translation entry having a divert flag set to use an alternative address to that held in the address translation entry.
- 9. (Original) The resource access control mechanism of claim 6, wherein the address translation mechanism is responsive to instigation of a diversion by the trap handler to set a divert flag in a translation entry of the address translation and is further operable to respond to a received address relating to an address translation entry having a divert flag set to modify an address held in the address translation entry.
- 10. (Original) The resource access control mechanism of claim 1, wherein the resource is at least one memory location.
- 11. (Original) The resource access control mechanism of claim 1, wherein the resource is a peripheral device.

12. (Original) The resource access control mechanism of claim 1, wherein the resource is a subsystem.

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- 13. (Currently amended) The resource access control mechanism of claim  $\underline{7}$  4, wherein the alternative resource is a faked response generator.
- 14. (Currently amended) The resource access control mechanism of claim  $\underline{7}$  4, wherein the alternative resource is a predefined memory portion.
- 15. (Original) A computer system comprising at least one processor that includes at least one central processing unit, memory, at least one peripheral device and a resource access control mechanism, wherein the resource access control mechanism comprises
  - an address translation mechanism operable to map a received address to a resource and
  - a trap handler for handling a trap in the event of a faulty resource access being detected, the trap handler being operable to instigate a diversion for subsequent access attempts to the resource and
  - the address translation mechanism being responsive to instigation of a diversion by the trap handler to effect the diversion for subsequent attempts to access the resource.
- 16. (Original) The computer system of claim 15, operable to identify an initial faulty access to a resource.
- 17. (Currently amended) A method of managing processor access to resources in a computer system, the method comprising:

a trap handler handling a trap in the event of an initial faulty access attempt to a resource being detected;

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defining said trap handler instigating a diversion in an address translation mechanism for subsequent access attempts to the same resource;

<u>said address translation mechanism</u> diverting a subsequent attempt to access the resource.

- 18. (Original) The method of claim 17, further comprising processing an exception.
- 19. (Original) The method of claim 17, wherein the defining of a diversion includes replacing a resource address held in an address translation entry for the resource with an alternative resource address.
- 20. (Original) The method of claim 17, wherein the defining of a diversion includes setting a divert flag in an address translation entry for the resource and the diverting of a subsequent attempt to access the resource includes using an different address to that held in the address translation entry when the divert flag is set.
- 21. (Original) The method of claim 17, wherein the defining of a diversion includes setting a divert flag in an address translation entry for the resource and the diverting of a subsequent attempt to access the resource includes modifying an address held in the address translation entry.
- 22. (Original) The method of claim 17, wherein the diversion is to a predefined memory portion.
- 23. (Original) The method of claim 17, wherein the diversion results in the generation of a faked response to the resource access.



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- 24. (Original) The method of claim 17, wherein the resource is at least one memory location.
- 25. (Original) The method of claim 17, wherein the resource is a peripheral device.
  - 26. (Original) The method of claim 17, wherein the resource is a subsystem.
- 27. (Original) A computer program on a carrier medium, the computer program forming a trap handler for a computer system and comprising computer code operable:

to respond to a faulty resource access by processing an exception; and

to instigate a diversion in an address translation mechanism for subsequent access attempts to the resource.

- 28. (Original) The computer program of claim 27, wherein the carrier medium is a storage medium.
- 29. (Original) The computer program of claim 27, wherein the carrier medium is a transmissions medium.

